11·20·01

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Attorney Docket No.: **Poly-17/APP**

Applicants: **Hung-Hsiang Jonathan CHAO, Eiji OKI**

Serial No.: **Not yet assigned**

Filing Date: **Herewith**

Title: **SCHEDULING THE DISPATCH OF CELLS IN MULTISTAGE SWITCHES**

Examiner: **Not yet assigned**

Group Art Unit: **Not yet assigned**

Assistant Commissioner for Patents
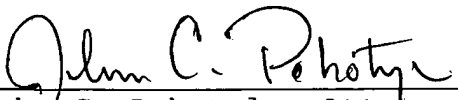**Box Patent Application**
Washington, D.C.   20231

S I R:

Information Disclosure Statement

The applicants respectfully request that the following references listed on the attached PTO-FORM-1449 be considered in the examination of the above-identified application. A copy of each of these references is enclosed.

The applicants preserve the right to establish that any of the references listed on the attached PTO-FORM-1449 are not prior art to the above-captioned application.

Respectfully submitted,

Dated: May 8, 2001

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-1-

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_____   36,242
John C. Pokotylo   Reg. No.

U.S. Department of Commerce Patent and Trademark Office			Complete if Known	
LIST OF REFERENCES CITED BY APPLICANT *(use as many sheets as necessary)*			Application Number:	Not yet assigned
			Filing Date:	Herewith
			First Named Inventor:	Hung-Hsiang Jonathan CHAO
			Group Art Unit:	Not yet assigned
			Examiner Name:	Not yet assigned
Sheet	1	of 1	Attorney Docket No.:	Poly-17/APP

OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume, issue number(s), publisher, country, where published, source	T[2]
	AA.	N. W. McKeown, "Scheduling Algorithms for Input-Queued Cell Switches", PhD Thesis, University of California at Berkeley, (1995).	
	AB.	C. Y. Lee and A. Y. Oruc, "A Fast Parallel Algorithm for Routing Unicast Assignments in Benes Networks", IEEE Trans. on Parallel and Distributed Sys., Vol. 6, No. 3, pp. 329-333 (March 1995).	
	AC.	T. T. Lee and S-Y Liew, "Parallel Routing Algorithms in Benes-Clos Networks", Proc. IEEE INFOCOM '96, pp. 279-286 (1996).	
r	AD.	N. McKeown, M. Izzard, A. Mekkittikul, W. Ellersick and M. Horowitz, "Tiny-Tera: A Packet Switch Core", IEEE Micro., pp. 26-33 (Jan-Feb. 1997).	
	AE.	T. Chaney, J. A. Fingerhut, M. Flucke, J. S. Turner, "Design of a Gigabit ATM Switch", Proc. IEEE INFOCOM '97, PP. 2-11 (April 1997).	
(	AF.	F. M. Chiussi, J. G. Kneuer, and V. P. Kumar, "Low-Cost Scalable Switching Solutions for Broadband Networking: The ATLANTA Architecture and Chipset", IEEE Commun. Mag., pp. 44-53 (Dec. 1997).	
	AG.	J. Turner and N. Yamanaka, "Architectural Choices in Large Scale ATM Switches", IEICE Trans. Commun., Vol. E81-B, No. 2, pp. 120-137 (Feb. 1998).	
	AH.	H. J. Chao and J-S Park, "Centralized Contention Resolution Schemes for a Large-Capacity Optical ATM Switch", Proc. IEEE ATM Workshop '97, (Fairfax, VA, May 1998).	
	AI.	N. McKeown, "The iSLIP Scheduling Algorithm for Input-Queued Switches", IEEE/ACM Transactions on Networking, Vol. 7, No. 2, (April 1999).	
	AJ.	N. McKeown, A. Mekkittikul, V. Anantharam, and J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch", IEEE Trans. on Communications, Vol. 47, No. 8, pp. 1260-1267 (Aug. 1999).	
	AK.	E. Oki, N. Yamanaka, Y. Ohtomo, K. Okazaki and R. Kawano, "A 10-Gb/s (1.25 Gb/s x 8) 4 x 2 0.25-μm CMOS/SIMOX ATM Switch Based on Scalable Distributed Arbitration", IEEE J. of Solid-State Circuits, Vol. 34, No. 12, pp. 1921-1934 (Dec. 1999).	
	AL.	J. Chao, "Saturn: A Terabit Packet Switch Using Dual Round-Robin", IEEE Communications Magazine, pp. 78-84, (Dec. 2000).	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Unique citation designation number. 2 Applicant is to place a check mark here if English language translation is attached.